Effects of Different Clock Gating Techinques on Design

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Abstract- Low power is one of the most important issues in today's ASIC (Application Specific Intregated Circuit) design. As the transistor is scaled down, power density becomes high and there is urgent need of reduction in power. The clock gating is one of the most elegant and classic techniques for reduction of power. Clock gating can be implemented by using any of these three cells, (1) Latch based cell (2) Flip-Flop based cell (3) Gate based cell. In this paper, we demonstrate the effect of different Clock Gating cells in design and how the design metrics, area, power and performance are affected for each clock gating cell. There are two variations in each clock gating cell, one is with Reset and other is without Reset. In this paper we also demonstrate how the design metric is affected by insertion of Reset signal in each Clock Gating cell.

Index Terms- Clock Gating, Application Specific Intregated Circuit, Very Large Scale Intregation.

1 INTRODUCTION

Achieving Low power is one of the most important issues in today's ASIC (Application Specific Intregated Circuit) design. As the transistor is scaled down, power density becomes high and there is an urgent need of reduction in power.

The synchronous design style is used by most of the designers now a days, in such synchronous circuits, most of the power is consumed in the clock network [1]. The clock network is responsible for flipping of the flip-flop (FF) and processing of the combinational logic.As the combinational logic does not oscillate much, it is the change in FF states that affects power consumption. The clock gating is one of the most vital techniques, which reduce clock network power [5]. By insertion of clock gating cells in a design, dynamic power as well as area occupied, are reduced. There are three ways to create a clock gating cell, these are (1) Latch based clock gating cell (2) FF based clock gating cell (3) Gate based clock gating cell [2].

We have used cadence RTL Compiler 10.1 for simulation. For modeling of wire delay, Physical Layout Editor (PLE) model is used with the following process corners [4].

1. Temperature -40C
2. Corner worst_low
3. Process SlowSlow
4. Voltage 0.95V

Due to this conservative modeling, Back hand results will not vary too much with Front hand results. For simulations, a 45nm low power digital library called nangateOpenCellLibrary_PDKv1_3_v2010_12 library is used.

All simulations are done on the design, openMSP430 which has the following features.

1. Interrupts: IRQ (x14), NMI (x1).
2. Power saving mode functionality.
3. Configurable memory size for both program and data.
4. Scalable peripheral address space.
5. Serial Debug Interface (Nexus class 3, w/o trace) with GDB support.
6. 16x16 hardware multiplexer.
7. Watchdog.
8. GPIO (General Purpose Input/Output) (port 1 to 6).

In this paper results are demonstrated for the frequency of 1 GHz, which is a very tight constraint for the design.

This paper makes the following contributions.

1. Analysis of effects of different CG cells on design metrics.
2. How the design metrics are going to change due to insertion of Reset signal in CG cell.

2. LATCH BASED CLOCK GATING CELL

2.1 Types

In latch based clock gating, latch is used as control element, it controls the Enable pin. In negative clock cycle, latch is allowed to reflect the change of Enable pin. In positive clock cycle, output of latch remains fixed. The high output of latch allows the clock to reach sequential logic. The period in which, we can sense the change in Enable signal is called active period, and other period in which we cannot sense the change in Enable signal is called sleep period. As shown in Fig. 1, negative half cycle of clock is active period, and positive half cycle is sleep period. If Enable signal changes during sleep period, the change of the Enable signal cannot be captured, this can lead to an incorrect design.

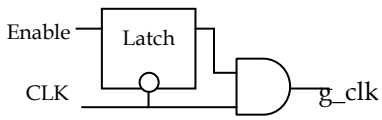

Fig. 1. Latch Based Clock Gating Cell

There are two types of Latch based clock gating cells. One is without Reset signal, which is shown in Fig. 1. Second is with

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Reset, which is shown in Fig. 2.

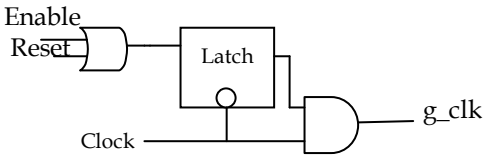

Fig. 2. Latch Based Clock Gating cell with Reset

2.2 Results & Analysis

The results for both the clock gating cells, is shown below in Table. 1.

TABLE 1
RESULT FOR LATCH BASED CG CELL WITH AND WITH-OUT RESET

Cell	Area (μm²)	Dynamic Power (nW)	Slack (ps)	
			Worst Negative Slack (WNS)	Total Negative Slack (TNS)
Latch Based CG Cell	32871.812	1628370.109	-239.3	-34851
Latch Based CG Cell with Reset	31140.188	1102700.774	-308.6	-55013

Insertion of Reset does not produce much effect on the design area; area is reduced by 5.2% only. The dynamic power is reduced by 32.28%, due to the reduction of switching activity at clock pin of sequential logic by Reset signal. But the TNS is increased by 57.85% due to the insertion of additional wire.

3. FF BASED CLOCK GATING CELL

3.1 Types

In FF based clock gating, FF is used as control element. When the negative edge of clock arrives, change of Enable will be reflected on FF output. If output of FF is high, clock is applied on sequential circuit. The sleep period is longer in FF based clock gating compared to Latch based clock gating. It means there is a greater chance to miss the change that happens on Enable signal.

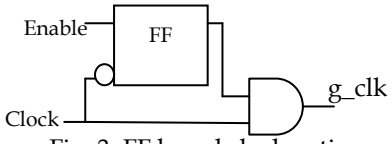

Fig. 3. FF based clock gating cell

There are two type of FF based clock gating cells. One is without Reset signal, which is shown in Fig. 3. Second is with Reset, which is shown in Fig. 4.

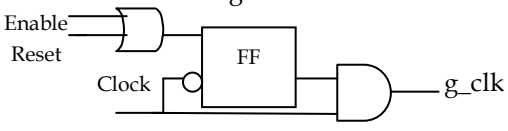

Fig. 4. FF based Clock Gating cell with Reset

3.2 Result & Analysis

Result for both clock gating cells, is shown below in Table.

TABLE 2
RESULT FOR FF BASED CG CELL WITH AND WITHOUT RESET

Cell	Area (μm²)	Dynamic Power(nW)	Slack (ps)	
			WNS	TNS
FF Based CG Cell	31851.357	1741111.98	-304.8	-41131
FF Based CG Cell with Reset	30996.302	962499.389	-326	-62193

Insertion of Reset does not produce much effect on design area; area is reduced by 2.6% only, however Reset signal reduces switching activity at sequential logic clock pin, due to which dynamic power reduces by 44.71%. But it increases TNS by 51.2071%. Increase of TNS has a detrimental effect on the performance of the design.

4. GATE BASED CLOCK GATING CELL

4.1 Types

This is one of the simplest ways to create a clock gating cell in the design. In Gate based clock gating, any gate is used for clock gating. In cadence RTL compiler, this technique is mentioned as None based clock gating and implemented by OR gate which is shown in Fig. 5 [2]. When the Enable is zero, output of the OR gate remain stable at logic '1', due to that no flipping will occur at the clock pin of sequential logic and there is no dynamic power consumption. If Enable is '1', output is same as the clock signal.

In this cell, there is no harm done due to sleep period as any time change in Enable signal will directly reflect on the output pin.

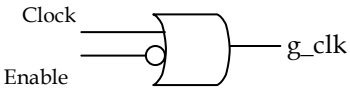

Fig. 5. Gate Based Clock Gating Cell

There are two types of Gate based clock gating cell. One is without Reset signal, which is shown in Fig. 5. Second is with Reset, which is shown in Fig. 6.

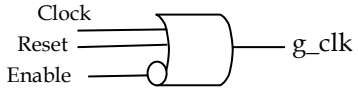

Fig. 6 Gate Based Clock Gating Cell with Reset

4.2 Result & Analysis

Results of both clock gating cells are shown below in Table. 3.

TABLE 2
RESULT FOR GATE BASED CG CELL WITH AND WITHOUT RESET

Cell	Area (μm²)	Dynamic Power (nW)	Slack (ps)	
			WNS	TNS
Gate Based CG Cell without Reset	32258.199	1442730.777	-286.2	-36546
Gate Based CG	32156.318	1047618.488	-311.3	-44196

Cell with Reset				

As can be seen from the Table. 2, the area of the design is slightly affected by insertion of Reset. Reset reduces the switching activity at sequential circuit clock port, due to which, dynamic power is reduced by 27.93%. However, insertion of Reset signal has a bad effect on the performance of the design. TNS is increased by 20.93%.

5. POWER & PERFORMANCE COMPARISON

5.1 CG Cells

The size of FF based CG cell is larger than the other CG cells. This requires large amount of capacitance to be charged and discharged in FF based CG cell during the switching. Hence, this design consumes highest dynamic power. The size of Gate based CG cell is smallest, so the dynamic power consumption is less in Gate based CG cell during switching due to the less amount of capacitance charging and discharging. Latch based CG cell consumes moderate dynamic power. Power comparison of different CG cells is shown in Fig. 7.

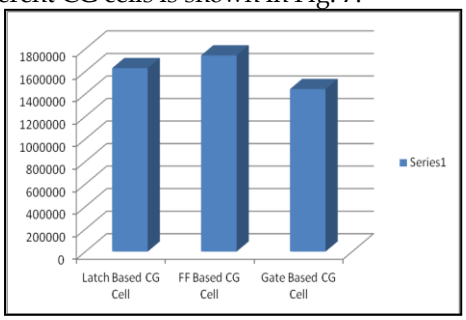

Fig. 7. Dynamic Power (nW) comparison of CG cells

Performance comparison of CG cell is shown in Fig. 8. We are judging the performance by TNS.The performance degrades with increase in the negative level of TNS. FF based CG cell having large amount of capacitance causes more delay in that cell, and hence the value of TNS is more in the FF based CG cell design.

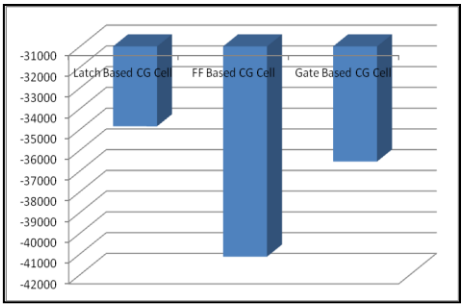

Fig. 8. TNS (ps) Comparison of CG cells

5.2 CG Cells with Reset Signal

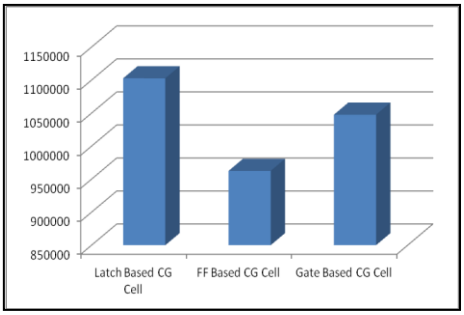

Fig. 9. Dynamic Power (nW) Comparison of CG Cells with Reset

Dynamic power in all CG cells is highly reduced by insertion of Reset. CG cell with Reset signal is more efficient in term of power reduction. Insertion of Reset in each clock gating cell will increase one wire in CG cells; capacitance and resistance of that wire affect the slack of the design. Here, we have estimated the slack by PLE model which calculates the slack based on resistance per unit-length and load per unit-length values. Due to this, TNS is high in CG cell with Reset in comparison to CG cell without Reset. Fig. 10 shows that CG cell with Reset is not efficient in terms of performance.

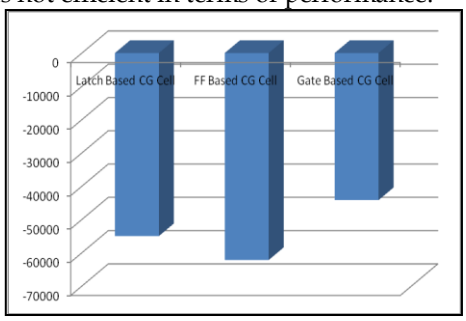

Fig. 10. TNS (ps) Comparison of CG cells with Reset

6. CONCLUSIONS

We have presented in-depth analyses of the effects of different CG cells on the design, as well as area, power and delay variations due to change in CG cells. When the constraint of power is more critical, Gate Based CG cell is more preferable. If the design is targeted for higher performance, Latch based CG cell is preferred. FF based CG cell is neither power nor performance efficient. Hence, the Latch based and Gate based CG cells are the only available good option for a designer. Power and Performance are not the only criteria, which are responsible for choice of a CG cell. There are some other parameters, which affect the selection of CG cell, those parameters are: i) sleep period and ii) glitches. In Latch based cell, there is a problem of sleep period, it means If Enable signal changes during sleep period, the change of the Enable signal cannot be captured, and that can lead to an incorrect design. The Gate based cell does not have this problem of sleep period, and so, it responds to changes in Enable irrespective of phase of clock.

The advantage of sleep period is that, there is no mismatch of delay between clock and Enable signal and this makes the design glitch free. Due to sleep period, problem of glitches is not found in Latch based CG cell. But the Gate based CG cell is affected by glitches, hence dynamic power goes high, but functionally everything is correct.

On the basis of switching activity factor of Enable signal which we can recover from VCD (value change dump) file [2], we can make the decision which CG cell is more appropriate for design. If the switching activity factor is high Gate based CG cell is more appropriate. If it is low, Latch based CG cell is more appropriate.

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